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Determination of the impact of the wire velocity on the surface damage of diamond wire sawn silicon wafers

Sindy Würzner^{a*}, Annemarie Falke^a, Rajko Buchwald^a, Hans Joachim Möller^a

^a*Fraunhofer THM, Am St.-Niclas-Schacht 13, Freiberg D-09599, Germany*

Abstract

The sawing of silicon wafers with diamond coated wires still requires further development for a widespread application in the photovoltaic industry. The technique has the potential for a cost reduction due to higher cutting rates and the use of water as a low-cost cooling fluid, but it is also necessary to integrate the technique into the established processing chains particularly for sawing multicrystalline silicon (mc-Si). One of the requirements is an increasing industrial demand on the wafer surface quality, such as the optical appearance, the total thickness variations (TTV), the etching behavior and the sub-surface and surface damage, which determines the mechanical wafer stability.

The goal of this work is to analyze the impact of different wire velocities on the surface damage of multicrystalline silicon wafers. First, the distribution of amorphous regions was measured using Raman microscopy. The results reveal slightly higher local fractions of the amorphous phase with increasing wire velocity. This also correlates with more scattering and higher inhomogeneity in the surface roughness values. Furthermore, the microcrack depths were analyzed on polished and etched bevel cut samples of wafers using confocal laser scanning microscopy (CLSM). Additionally, the present study investigates the impact of cleaning procedures and different grain orientations on the sawing damage characteristics.

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Keywords: Diamond wire; silicon; wire velocity; surface damage; microcrack depth; material stress; amorphous phase; surface roughness

* Corresponding author. Tel.: +49 3731 2033 164; fax: +49 3731 2033 199.

E-mail address: sindy.wuerzner@thm.fraunhofer.de

1. Introduction

The diamond wire sawing technology on the basis of fixed abrasive grains is a promising alternative to the standard slurry based method with loose abrasive particles [1]. The production of silicon wafers with diamond-plated wire offers a cost reduction due to higher cutting rates, economy of wire and the application of water as low-cost cooling fluid. At the same time, the quality of the wafer surface has to be maintained at least. However, a main goal for further development of higher sawing performances by means of diamond-plated wire is a significant improvement of the wafer surface and sub-surface. The degree of saw damage is a crucial factor because of the impact on the wafer stability. An enhancement of the wafer stability requires a substantial reduction of the surface damage.

During the sawing, mechanical stresses induced by the wire, act upon the wafer surface. The degree of the surface damage is influenced by the sawing process parameters. One of these is the wire velocity. Furthermore the crystallography of the silicon has an impact on the surface damage due to the crystal orientation dependency of the crack depth [2]. In the present work Raman spectroscopic analyses was carried out on wafers, which were sawn with varying wire velocities. The distribution of material stresses and the possible phase transformations of surface regions have been investigated in detail. A systematic method to determine the ratio r of amorphous to crystalline silicon on the wafer surface was established to gather information on ductile cutting of silicon ingots. Also the influence of the cleaning process on the wafer surface was investigated. Furthermore, the surface roughness as well as the depth distribution of microcracks on polished etched bevel cut samples taken from the wafers were determined using confocal laser scanning microscopy (CLSM). In particular, the influence of the process parameter – wire velocity – on the surface quality has been analyzed in these investigations.

Nomenclature

r	Raman intensity ratio of amorphous to crystalline silicon
S_a	Average roughness [μm]
S_v	Maximum valley depth [μm]
S_p	Maximum peak height [μm]
S_k	Core roughness depth [μm]

2. Sample description

To characterize the surface induced by industrial diamond wire sawing, standard cleaned mc-Si wafers were produced using three different wire velocities: slow – 5 m/s, middle – 10 m/s and fast – 15 m/s. The silicon ingot is pushed against the wire web with a constant feeding rate which is equal to the sawing rate. During acceleration and deceleration the feed speed is proportionally adapted to the wire velocity. The higher sawing velocities result however in lower forces acting in sawing direction (see Fig. 1). One wafer of each sawing process was examined.

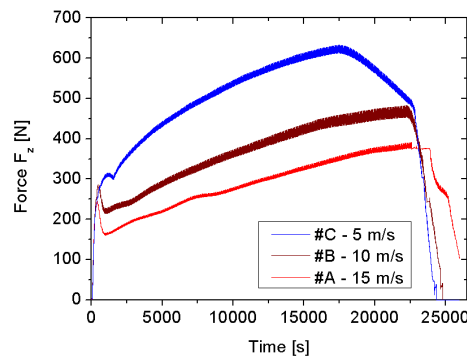


Fig. 1. Force-time diagram of diamond wire sawing with three different wire velocities. Shown is the total force in sawing direction (F_z).

For reference analysis of the impact of the cleaning process on the wafer surface two neighboring monocrystalline silicon (cz-Si) wafers – as-sawn and cleaned – were investigated. These wafers have been sawn under similar conditions with a wire velocity of 15 m/s. The wafer surfaces were analyzed regarding material stresses, phase changes and surface roughness. Neighboring wafers were used to prepare polished and etched bevel cut samples to study the microcrack depth. Wafer areas were hereby polished with an angle of 1° to lay bare damage structures lying underneath the surface. Table 1 provides an overview of the measured wafers/samples and gives additional information, which analyses were performed.

Table 1. Overview of measured wafers/samples and analyses.

Wafer/sample and description	Wire velocity	Analysis		
		Raman intensity ratio	Surface roughness	Crack depth
#A: wafer mc-Si clean	15 m/s	X	X	
#B: wafer mc-Si clean	10 m/s	X		
#C: wafer mc-Si clean	5 m/s	X	X	
#D: wafer cz-Si clean	15 m/s	X		
#E: wafer cz-Si as-sawn	15 m/s	X		
#bsA1: sample of grain orientation z{111}	15 m/s	X	X	X
#bsA2: sample of grain orientation z{211}	15 m/s	X	X	X
#bsC1: sample of grain orientation z{111}	5 m/s	X	X	X
#bsC2: sample of grain orientation z{211}	5 m/s	X	X	X

3. Experimental procedure

3.1. Raman spectroscopy

With dispersive Raman spectroscopy and microscopy the distribution of material stresses and crystalline or other phases can be measured with high spatial resolution. Specifically, it is possible to detect tensile and compressive stresses as well as the distribution of amorphous silicon layers. The Raman mappings were performed using an excitation laser with a wavelength of 532 nm and a resulting laser power of 1.2 mW on the sample surface.

To evaluate the amorphous silicon fraction on the wafer surfaces a special averaging method was applied. The measured single Raman spectra belonging to one map were summed up to improve the signal-to-noise deviation. One sum spectrum contains up to 2400 single Raman spectra. According to Yan et al. [3], the ratio r of amorphous to crystalline silicon allows conclusions about the thickness of the amorphous layer on a wafer surface. The amount of material is proportional to the intensity of the Raman line, or the area under the respective Raman curve. In order to isolate the crystalline and amorphous peaks, the sum spectrum has been fitted with a number of single curve fits. The crystalline peak at approximately 520 - 521 cm^{-1} was fitted using a Lorentzian distribution. The peaks indicating amorphization were fitted with Gaussian distribution. The most intense main peak of the amorphous phase lies at 470 - 480 cm^{-1} . With the parameters peak height h_a and h_c as well as peak half power band width b_a and b_c of the amorphous and crystalline peak fits, the ratio r was calculated using equation (1). Yan et al. [3] also presented a theoretical relation between r and the depth of the amorphous layer d_a given in equation (2).

$$r = \frac{h_a \cdot b_a}{h_c \cdot b_c} \cdot \frac{1}{\sqrt{\pi}} \quad (1)$$

$$d_a = 33.3 \cdot \ln \left(\frac{8.84 + 15 \cdot r}{8.84 + 0.167 \cdot r} \right) \quad (2)$$

3.2. Confocal laser scanning microscopy

Further characterization of the wafer quality was performed with a confocal laser scanning microscope. With this method the surface roughness was measured by means of 3D surface parameters according to DIN EN ISO 25178-3:2008-03 [4]. A cut-off wavelength for the L-filter of 40 μm was chosen. The S-filter was set to 0.12 μm . To determine all surface parameters for the analysis done here, a map of 3 x 3 images was taken at the same positions as used for Raman analysis. Each picture had a size of 43 x 43 μm^2 . There are different roughness parameters for the 3D analysis of surfaces. Amplitude parameters giving information about the various texture features of the surface, for example S_a , S_v and S_p . The average roughness S_a gives the arithmetic mean of the absolute ordinate values. The maximum valley depth S_v and the maximum peak height S_p are defined as the lowest and highest point of the measured surface area. Function-oriented parameters, for example S_k , can be derived from the bearing area curve also known as Abbott-Firestone curve. The core roughness depth parameter S_k indicates the distance between highest and lowest point of the so called surface core.

The depth of microcracks resulting from the abrasive process during diamond-plated wire sawing was also determined using CLSM, by analyzing bevel cut samples. Therefore, the specimens were mechanically polished perpendicular to the saw marks with a slight inclination of 1° to the original sawn damaged sample surface, followed by a Secco etching. On the polished and etched beveled part of the sample the damage structure with microcracks becomes laid open and visible on the surface. The microcracks gradually vanish with increasing polished sample depth. To determine which microcrack runs deepest into the sample depth, the microcrack traces from the original sample section to the bevel polished surface were taken by micrography and measuring the surface profiles parallel to the sawing marks. Subsequently the height difference between the original sample height and the height, at which the last microcrack is found, is registered.

3.3. Laue scanner

The determination of the grain orientation was carried out by using of the Laue scanner system, which is based on X-ray diffraction. Depending on the orientation of the grain, the white X-ray beam generates a backscatter diffraction pattern of all possible lattice plane families. With this Laue pattern an orientation matrix with Euler angles is calculated, which transforms the crystal axes of the individual grain lattices to the sample-fixed coordinate system. More details on the Laue scanner method can be found in ref. [5].

3.4. Cleaning process for silicon wafer

In general, the silicon wafers are cleaned directly after sawing by wet chemical standard cleaning steps. Through the cleaning process the wafer surface is removed of particles and chemical impurities. The procedure consists of several cleaning tanks and includes the cleaning with a solution of an alkaline medium as well as the rinsing with demineralized water. All steps are carried out under thermal-alkaline ultrasonic cleaning with different frequencies.

4. Results and discussion

4.1. Surface amorphization and material stresses

• Impact of wire velocity

To get an overview over the amount of and any possible dependence on the sawing velocity, three wafers sawn with different wire velocities were evaluated regarding their amorphous silicon fraction. Using Raman spectroscopy a total area of 2.7 x 1.8 mm^2 made up of evenly distributed areas was measured on each wafer.

Fig. 2 depicts Raman sum spectra obtained from a single map of wafer #A, #B and #C each. The red line resembles a Raman curve measured on the surface of a wafer sawn with high wire velocity of 15 m/s; the blue line gives the trend of a Raman curve acquired from a slowly sawn wafer surface of 5 m/s and the brown graph gives the Raman spectrum of a wafer sawn with a medium velocity of 10 m/s. As a reference an etched wafer free of damage

and therefore only containing crystalline silicon was used and is given by the green graph. Unstrained crystalline silicon (c-Si) exhibits a Raman peak at 521 cm^{-1} , the main peaks at 470 cm^{-1} and 150 cm^{-1} imply the presence of amorphous silicon (a-Si) [6]. The results of Fig. 2 reveal a slightly higher fraction of amorphous silicon on the fast sawn wafer. This can be explained by considering the behavior of silicon under stress [7]. Under high pressure, the material undergoes a phase transition to a phase with metallic characteristics. Upon pressure relief a further phase transition takes place depending on the relief velocity. At a slow relief, a mixture of crystalline phases is produced. If the pressure relief occurs fast, the silicon becomes amorphous, i.e. fast sawn wafers will exhibit a higher ratio of amorphous to crystalline material compared to slowly sawn ones. This can be seen in the r -values. The evaluation of r was carried out according to the equation (1) and of the amorphous layer thickness via equation (2).

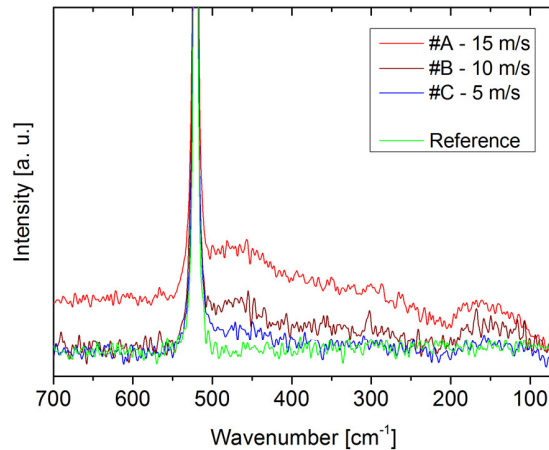


Fig. 2. Raman sum spectra of small wafer surface areas sawn with different wire velocities.

The amorphous to crystalline ratio r results in a median of 0.28 for the fast sawn wafer #A and 0.17 for the slowly sawn wafer #C. On average this corresponds to a present amorphous layer of 12.8 nm (wafer #A) and 8.3 nm (wafer #C). But it is noticeable, that the single r -values are strongly scattered with a minimum value close to 0 (parts nearly without amorphous silicon) being found on each wafer and a maximum of 0.54, which was only found on the fastest sawn wafer. This implies that the wafer surfaces mostly consist of randomly scattered amorphous fractions. From these results, it cannot reliably be concluded whether the value for r is clearly dependent on the wire velocity.

The acquired maps were also evaluated regarding the Raman shift of the crystalline silicon peak due to residual stresses in the silicon material. Note that a peak shift towards lower wave numbers indicates tensile and to higher wave number compressive stress. The peak shifts have been calibrated in ref. [6] and show that a difference of 3.2 cm^{-1} corresponds to a stress of 1 GPa. Fig. 3 gives an example of Raman maps showing the crystalline peak shift acquired from fast sawn wafer #A and slowly sawn wafer #C. It is apparent that the sawing induced surface pattern is also resembled in the spatially mapped wave number of the crystalline silicon peak found on all measured wafers. The wave number maps show local tensile stresses resulting in peak downshifts up to 517 cm^{-1} and compressive stresses in peak upshifts up to 525 cm^{-1} . This implies tensile and compressive stresses of up to 1.25 GPa. In comparison to the slowest sawn wafer (Fig. 3b), a more inhomogeneous stress distribution (compressive and local tensile stress) is present on the fastest sawn wafer (Fig. 3a). This can also be observed by the Raman maps of the half power band width of the crystalline silicon peak (not shown here).

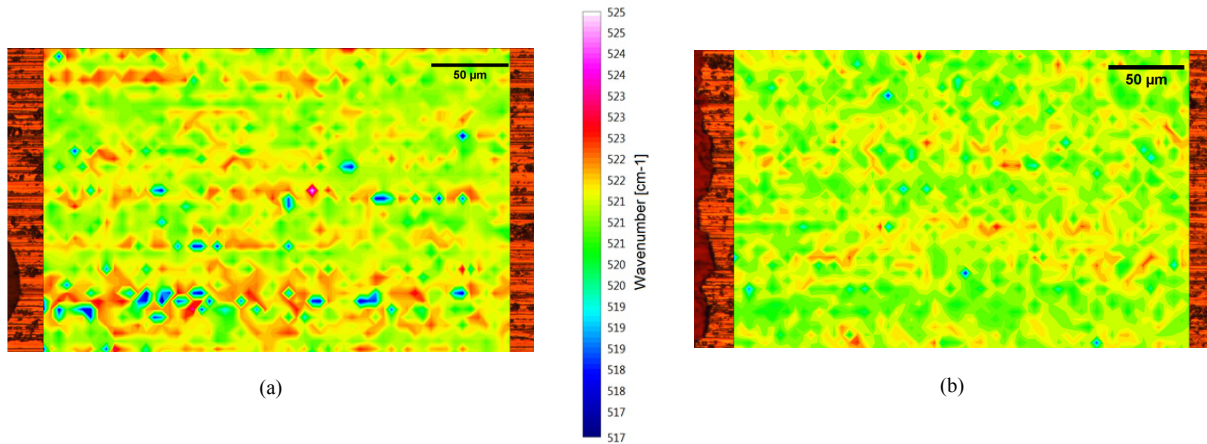


Fig. 3. Raman map from fastest sawn wafer #A (a) and slowest sawn wafer #C (b) showing the wavenumber of the crystalline silicon peak.

- Impact of cleaning procedure

In order to analyze possible effects of the cleaning process on the wafer surface, two neighboring wafers, one cleaned (wafer #D) and one as-sawn (uncleaned, wafer #E), were investigated. These are monocrystalline wafers, which have been sawn under similar conditions with a wire velocity of 15 m/s. To analyze the surfaces, the ratio r of amorphous to crystalline material was determined for both wafers.

Spectra obtained from single points on the Raman map are given in Fig. 4. Here, two spectra from each wafer are compared. The green and blue curves represent spectra obtained from the as-sawn wafer #E. The amorphous peaks at 470 cm^{-1} and 150 cm^{-1} are more distinct than in the orange and red curve obtained from the cleaned neighboring wafer #D. The ratio r of amorphous to crystalline silicon results in a median of 0.27 for the cleaned wafer #D and 0.71 for the as-sawn wafer #E. Thereby the thickness of the amorphous layer found on the as-sawn wafer #E is with 25.9 nm much higher. This leads to the assumption, that by cleaning the wafer surface, a large part of the amorphous material is removed. This could be, because the cleaning process acts as an etchant which attacks the amorphous phase on the surface. From the results it can be calculated that by chemically cleaning the wafer surface, the amorphous layer is reduced by approximately 50 % on average.

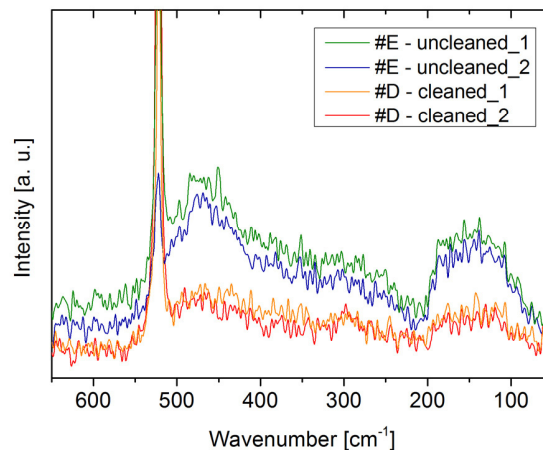


Fig. 4. Raman spectra acquired from as-sawn and cleaned multicrystalline wafer surfaces.

4.2. Surface roughness determination

Surface roughness measurements have been made on the same wafer areas where Raman maps have been carried out. Parts with an increased amount of chipped areas and more pronounced saw grooves showed increased roughness values. Fig. 5 gives optical confocal laser microscope images of two wafer surface areas sawn with different wire velocities. The sawing marks induced by the diamond wire sawing are visible on both wafers. These grooves are accompanied by chipped parts. However, the surface of wafer #A sawn with higher wire velocity is more inhomogeneous rough in comparison to the slowest sawn wafer surface #C. This correlates with the previously established fact of a more inhomogeneous distribution of tensile and compressive stresses on the fastest sawn wafer surface. A relationship between the surface roughness parameters and the amorphous to crystalline silicon ratio r could not be found.

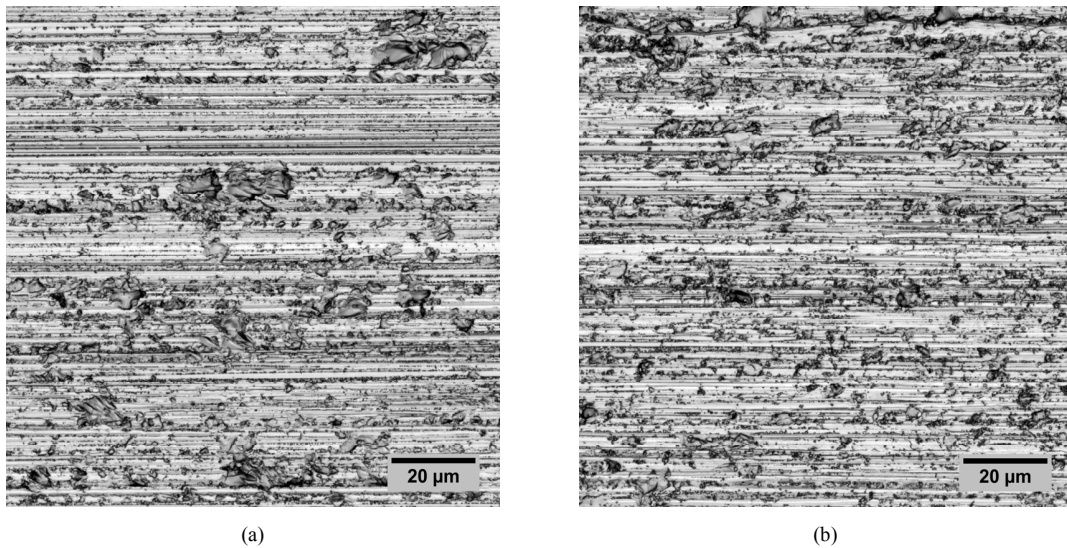


Fig. 5. CLSM images of a section of fast (a) and slowly (b) sawn wafer surface (wafer #A and wafer #C).

The obtained confocal microscope images were evaluated concerning the surface roughness parameters. Here three parameters, S_a , S_v and S_k , are singled out. The resulting values are given in the box plots of Fig. 6. Two wafer surfaces (#A – 15 m/s and #C – 5 m/s) were compared. In general, it was found that the range of fluctuation of the surface roughness values increases for the fastest sawn wafer #A and thereby also the inhomogeneity increases. But the mean value and the median of the surface roughnesses are slightly higher for the slowest sawn wafer #C. However, minimal roughness values are found on the fast sawn wafer #A.

The amplitude parameter S_a ranges from 0.08 to 0.17 μm (median 0.14 μm) for the fast sawn wafer #A and from 0.12 to 0.18 μm (median 0.16 μm) for the slow sawn wafer #C. Also, the values for the amplitude parameter S_v , which characterize the valley depth of a sample surface, scattered over a large range at high sawing velocity (0.76 - 2.51 μm with a median of 1.29 μm). For the slowly sawn wafer, the obtained values lie further together (1.05 - 1.57 μm with a median of 1.33 μm). The parameter of the total peak height S_p (not shown here) leads to a similar behavior (#A: 0.53 - 1.25 μm , median 0.74 μm / #C: 0.66 - 1.14 μm , median 0.93 μm). This means that fast sawing results in surfaces with higher peaks and lower valleys than those of slowly sawn wafers. Valleys could be sawing grooves or chipped areas. Peaks could be formed by residual material found on the flanks of the sawing marks. For the core roughness depth S_k values were determined between 0.22 and 0.43 μm (median 0.36 μm) as well as between 0.36 and 0.50 μm (median 0.43 μm) for the fast and slowly sawn wafer.

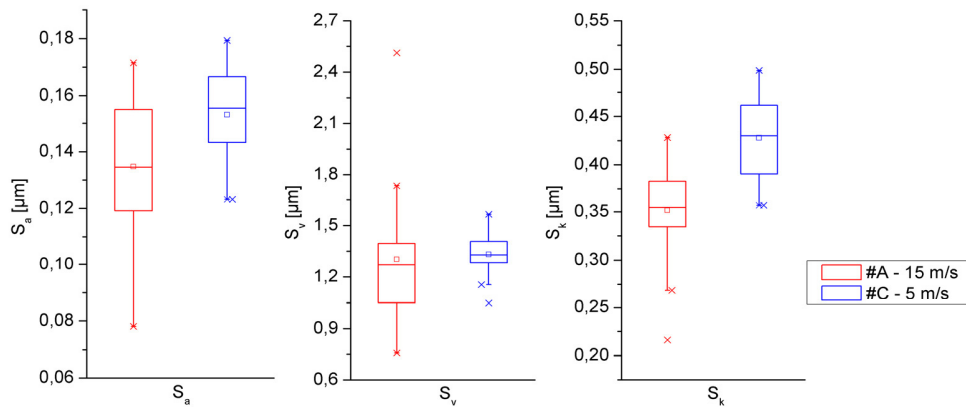


Fig. 6. Box charts of the 3D surface parameters S_a , S_v and S_k for wafer surfaces sawn with different wire velocities.

4.3. Microcrack depth analysis

The maximum microcrack depths of as-sawn multicrystalline silicon wafers were measured using CLSM. For this purpose, polished and etched bevel cut samples were prepared of selected individual grains of a fast and slow sawn neighboring multicrystalline wafer. Two grain orientations were observed: surface normal orientation in z of $\{111\}$ and $\{211\}$.

Fig. 7 presents the box plot of the results of this crack depth analysis. Generally, the microcrack depths scattered between values of $2\text{ }\mu\text{m}$ and $13\text{ }\mu\text{m}$. The median obtained for the $\{211\}$ plane increases from $3.9\text{ }\mu\text{m}$ for the fast sawn wafer sample #bsA2 (orange box plot) to $5.2\text{ }\mu\text{m}$ for the slower sawn wafer sample #bsC2 (light blue box plot). The difference in median and maximum of the crack depth for the $\{111\}$ plane is very small, but show a similar trend (see red and blue box plot). These results imply, that the faster the wire velocity the lower the subsurface damage by microcracks. This correlates with lower forces in sawing direction for higher velocities due to the constant feed rate. Higher wire velocities could induce more material removal in wire sawing direction, so that lower depth damage is caused. A dependency between the grain orientation, at least for the $\{111\}$ and $\{211\}$ planes, and the microcrack depth is not evident. However, prior investigations on three different crystal orientations ($\{100\}$, $\{101\}$ and $\{111\}$) have shown a clear correlation to the crack depth [2]. The median of the maximum crack depth was lowest for the $\{100\}$ plane and highest for the $\{111\}$ plane.

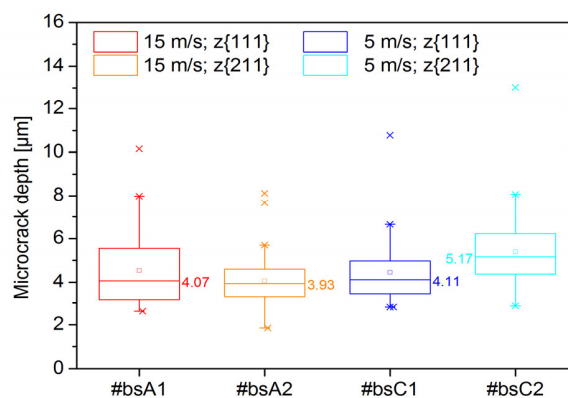


Fig. 7. Box charts of the measured microcrack depth. Two samples were taken from fast sawn wafer #A and two samples from slowly sawn wafer #C with surface normal orientation $\{111\}$ and $\{211\}$.

5. Conclusion

The aim of this work was to analyze the impact of different wire velocities (5, 10 and 15 m/s) on the surface damage of multicrystalline silicon wafers (the silicon ingot feed rate during the sawing process was kept constant). Therefore measurements of the Raman intensity ratio r of amorphous to crystalline, material stresses, surface roughness and crack depth were performed.

The results reveal a slightly increased fraction of amorphous silicon on the faster sawn wafer. This could be explained by the behavior of silicon under fast pressure relief. Further investigations are required because of the variations in the r -values. In comparison to the slowest sawn wafer, a more inhomogeneous stress distribution with compressive and local tensile areas is present on the fastest sawn wafer. This correlates with the more inhomogeneous surface roughness at higher wire velocity. Generally, parts with an increased amount of chipped areas and more pronounced saw grooves showed increased surface roughness values. The wafers sawn with higher wire velocity revealed more fluctuations in the surface roughness values and increased inhomogeneity. No relation was found between the surface roughness parameters and the amorphous to crystalline silicon ratio r .

The influence of a standard cleaning step after sawing on the wafer surfaces has been investigated. It was observed that by our cleaning procedure approximately 50 % of the amorphous silicon surface layer present after sawing is etched away by the chemical process. This corresponds to an average layer thickness of about 13 nm. This may explain, why in literature contradictory results regarding the occurrence of amorphous regions after diamond wire sawing have been reported.

Furthermore, the microcrack depth was analyzed on fast and slowly sawn multicrystalline silicon wafer samples with two different grain normal orientations: $\{111\}$ and $\{211\}$. The wire velocity seems to have an effect on the microcrack depth. Results show that a faster wire velocity leads to lower values of the maximum crack depth which correlates with lower forces acting in sawing direction. First investigations on monocrystalline silicon material support this result.

All results of the current investigations are again summarized in Table 2.

Table 2. Overview of the measured results. All values indicate the median.

Wafer/sample and description	Wire velocity	Analysis		
		Raman intensity ratio r	Surface roughness S_a / S_v / S_k	Crack depth
#A: wafer mc-Si clean	15 m/s	0.28	0.14 / 1.29 / 0.36 μm	
#B: wafer mc-Si clean	10 m/s	0.20		
#C: wafer mc-Si clean	5 m/s	0.17	0.16 / 1.33 / 0.43 μm	
#D: wafer cz-Si clean	15 m/s	0.27		
#E: wafer cz-Si as-sawn	15 m/s	0.71		
#bsA1: sample of grain orientation $z\{111\}$	15 m/s	0.24	0.15 / 1.23 / 0.43 μm	4.07 μm
#bsA2: sample of grain orientation $z\{211\}$	15 m/s	0.26	0.09 / 0.88 / 0.27 μm	3.93 μm
#bsC1: sample of grain orientation $z\{111\}$	5 m/s	0.15	0.12 / 1.08 / 0.37 μm	4.11 μm
#bsC2: sample of grain orientation $z\{211\}$	5 m/s	0.15	0.14 / 1.16 / 0.42 μm	5.17 μm

A further systematic investigation of the surface damage of diamond wire sawn monocrystalline silicon wafers depending on the wire velocity is in progress. With this analysis on monocrystalline material the possible impact of the grain orientation on the scattering of the Raman signal should be excluded. The range of the wire sawing velocity could be extended.

Acknowledgements

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